A 800 MHz Fully Synthesizable PLL with Calibration-Free Feedforward Noise Cancellation

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***Summary*— A novel calibration-free feedforward noise cancellation (FNC) scheme for cell-based synthesizable all-digital phase locked loop (ADPLL) is presented. FNC is realized by selecting the ring-oscillator (RO) phase closest to the reference edge as the output clock on each reference cycle. We present an analytical model for FNC performance based on the frequency domain analysis on different noise sources. Fabricated in 65nm 1.2-V CMOS technology, the cell-based ADPLL layout is done by an automatic place and route (APR) tool except for the 2 auxiliary cells comprising the DCO. Measurement results show that the novel feedforward scheme suppresses in-band phase noise by 15 dBc/Hz, and integrated rms jitter by 4.22x with only 0.25mW of additional power consumption when the contribution of DCO random noise dominates TDC quantization noise. However, on the opposite case (TDC noise > DCO noise), the feed-forward scheme increases the out-of-band noise and rms jitter. The frequency domain analytical model predicts this tendency of the measurement results. We propose a condition for the feed forward scheme to be beneficial based on the analytical model and simulation results. (*Abstract*)**

Keywords—PLL, Synthesizable PLL, Feedforward, Frequency Synthesizer (*key words****)***

I. INTRODUCTION

Ring oscillator (RO) based phase locked loops (PLLs) have compact area, better compatibility with digital circuits, and require less design effort compared to LC-PLLs. The use of RO also enables cell-based architecture, which can be built with automatic place and route (APR) tool, reducing design and porting effort [1]. However, poor phase noise (PN) performance and supply sensitivity of ROs limit the PLL performance. One of the techniques to compensate for the RO performance is feedforward noise cancellation (FNC) [2-3]. By feeding forward the phase error captured by the phase detector to the output clock, FNC reduces the noise level of the PLL without affecting the stability. Fig. 1 shows 2 different architectures of previously published FNC PLLs. [2] uses a delay-line discriminator (DD) embedded in the RO to extract the out-of-band PN and cancels the noise component using a voltage-controlled delay (VCD) element outside of the PLL. [3] uses a sub-sampling phase detector (SSPD) to capture the phase error and uses its output voltage to control the VCD. Both [2] and [3] achieved >10dBc/Hz PN suppression with FNC. However, since the controllable delay unit that cancels the noise is separate from the noise detection unit, both require gain calibration of the FNC path for accurate cancellation. We propose an FNC method that does not require any calibration, and is amenable to cell-based design and APR. The structure of the brief is as follows. First, in Section II, the architecture of the proposed ADPLL and the frequency domain analysis of the FNC effect on different noise sources are explained. In Section III, implementation details are introduced, and the measurement results are evaluated. Section IV presents the conclusion.

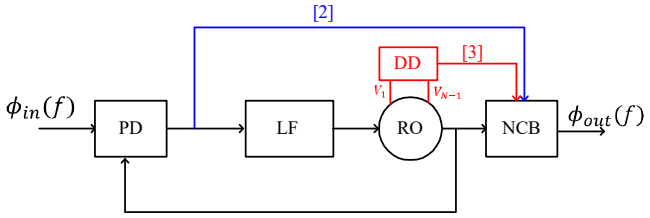


Fig. 1. Block diagram of the proposed synthesizable PLL with edge selection FNC technique.

II. EDGE SELECTING FEEDFORWARD NOISE CANCELLATION

A block diagram of the proposed feedforward ADPLL is shown in Fig. 2. The baseline architecture is adapted from [4]. The phase information of the DCO is captured by an embedded TDC and digital counter. The embedded TDC quantizes the node voltages of each stage of the DCO on the rising edge of the reference clock, capturing the fractional phase error [5]. In our design, 8 differential phase interpolators double the 16 phases of the differential DCO to 32, quantizing the fractional phase error into 5-bits.

Fig. 3 shows a signal diagram of edge selection logics. Initially, CK_OUT is connected to *PH[0]*. But on the next rising edge of CK_REF, due to DCO noise, *PH[3]* is the closest edge to CK_REF instead of *PH[0]*. This information is captured by embedded TDC, latching *PH[3]*=1 and *PH[4]*=0. Using this information, the code of the edge selection block, EDGE_SEL, gets updated on the retimed CK_REF, which is approximately 4 DCO cycles after the reference edge. The edge selection block selects *PH[3]* as the output clock,

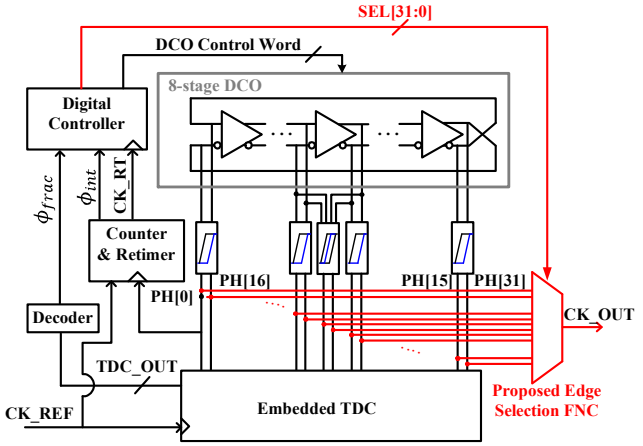


Fig. 2. Block diagram of the proposed synthesizable PLL with edge selection FNC technique.

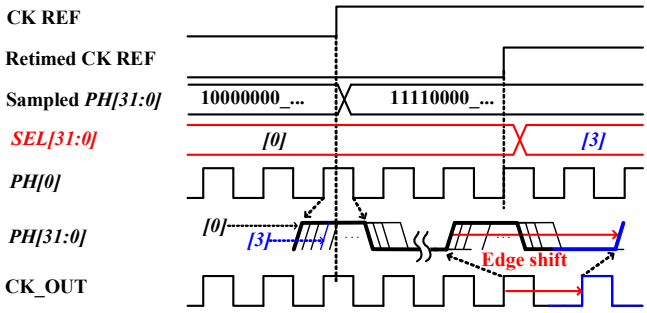


Fig. 3. Timing diagram of the proposed edge selection FNC process.

instantaneously reducing the phase error by $3\Delta T_{tdc}$, where ΔT_{tdc} is the time resolution of the TDC.

One drawback of both the embedded TDC and the proposed FNC scheme is the quantization noise due to this finite time resolution; $\Delta T_{tdc} = T_{dco}/N_{tdc}$, where T_{dco} is the period of the DCO clock, and N_{tdc} is the number of phases that the TDC latches (32 in the proposed design). The TDC resolution adds quantization noise into the loop and the FNC path, degrading the PN performance of the PLL.

Fig. 4 illustrates a linearized phase domain model of the proposed PLL with different noise sources. The term main path (MP) and FNC path (FNCP) will be used to indicate each output of the normal PLL loop and the feedforward path. $\phi_{pll_{out}}$ is the output phase of MP, which is sampled by the reference clock on every phase comparison event. In the frequency domain, this generates a train of copied spectra with f_{ref} spacings (red graphs). The loop filter in the MP suppresses these copied spectra while the FNCP only has filtering by zero-order hold (ZOH) action, which transfer function is

$$H_{ZOH}(f) = e^{-i\pi f T_{ref}} sinc(f T_{ref}), \quad (1)$$

where $T_{ref} = 1/f_{ref}$. Since $H_{ZOH}(s)$ has $1/f^2$ roll off, it suppresses the out-of-band spectra, but not as sharp as the MP does, which transfer function is

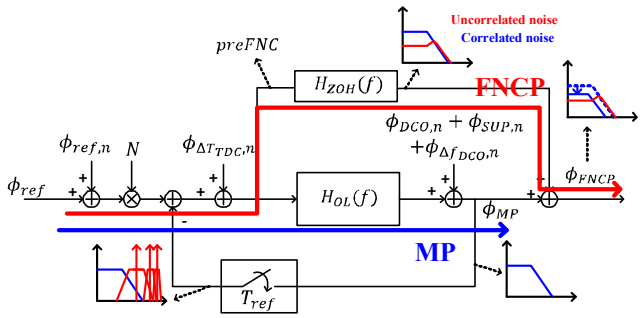


Fig. 4. Linearized phase domain model of the FNC technique.

$$H_{OL}(f) = \left(K_p + \frac{K_i}{1-z(f)^{-1}}\right) \cdot z(f)^{-1} \cdot H_{ZOH}(f) \cdot \frac{K_{DCO}}{1-z(f)^{-1}} \quad (2)$$

where $z(f)^{-1} = exp(-i2\pi f/f_{ref})$. Based on (1) and (2), below three subsections analyze the FNC effect on different noise sources.

A. DCO noise shaping

In the following analysis, DCO noise implies the sum of 1) DCO random noise, $\phi_{DCO,n}$, 2) DCO phase deviation due to supply noise, $\phi_{SUP,n}$, and 3) DCO phase deviation due to DCO frequency resolution, $\phi_{\Delta f_{DCO},n}$. $S_{\phi,DCO,n}(f)$ indicates the noise spectrum of DCO noise. The PN spectrum of the PLL output due to DCO noise is then expressed as

$$S_{\phi,MP}(f)|_{DCO,n} = S_{\phi,DCO,n}(f) \cdot \frac{1}{1+H_{OL}(f)}. \quad (3)$$

The copied spectra generated from sampling action are not correlated with $\phi_{pll_{out}}(f)$. Thus, the FNCP adds uncorrelated noise shaped by $|H_{ZOH}(f)|^2$ while cancelling the correlated portion shaped by $|1 - H_{ZOH}(f)|^2$ [6]. Sum of the two is expressed as

$$S_{\phi,FNCP}(f)|_{DCO,n} = |1 - H_{ZOH}(f)|^2 \cdot S_{\phi,MP}(f)|_{DCO,n} + |H_{ZOH}(f)|^2 \cdot \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,MP}(f - k \cdot f_{ref})|_{DCO,n}. \quad (4)$$

Because the high frequency suppression of $|H_{ZOH}(f)|^2$ is less sharper than $|H_{OL}(f)|^2$, FNCP adds out-of-band noise to the MP. Fig. 6(a) and (b) show a PN break-down of MP and FNCP, showing this DCO noise shaping of both paths. But the amount of noise cancelled by the FNCP is much larger than the added, reducing the overall jitter from DCO and power supply.

B. TDC quantization noise shaping

Assuming white noise, the single-sided TDC quantization noise spectrum can be expressed as

$$S_{\phi,TDC,n}(f) = \frac{(2\pi)^2}{12}\left(\frac{\Delta T_{TDC}}{T_{DCO}}\right)^2 \frac{1}{f_{ref}}. \quad (5)$$

The PN spectrum of MP due to TDC quantization is then expressed as

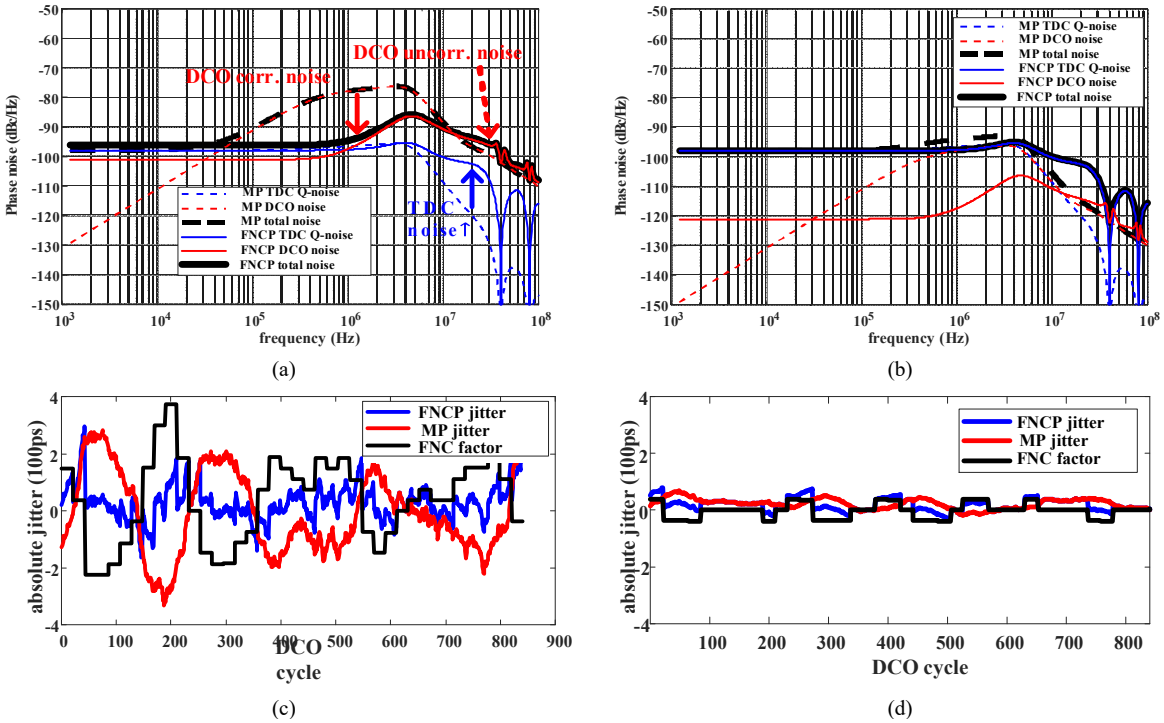


Fig. 5. Performance comparison of MP and FNCP in two different environments. PN plots when (a) DCO noise dominates, (b) TDC noise dominates. Time domain simulation plot when (c) DCO noise dominates, (d) TDC noise dominates

$$S_{\phi,MP}(f)|_{TDC,n} = S_{\phi,TDC,n}(f) \cdot \frac{H_{OL}(f)}{1+H_{OL}(f)}. \quad (6)$$

The spectrum of TDC noise at node *preFNC* is then

$$S_{\phi,preFNC}(f)\big|_{TDC,n} = S_{\phi,TDC,n} \cdot \frac{1}{1+H_{OL}(f)}. \quad (7)$$

The transfer function of the correlated path of FNCP for $S_{\phi,MP}(f)|_{TDC,n}$ is then

$$\frac{\phi_{FNCP,corr.}}{\phi_{MP|TDC,n}} = \left|1 + \frac{H_{ZOH}(f)}{H_{OL}(f)}\right|^2. \quad (8)$$

Unlike the transfer function of the DCO's correlated path in (4), (7) adds noise instead of cancelling it. Intuitively, since $S_{\phi,preFNC}(f)\big|_{TDC,n}$ is a high-passed spectrum of $S_{\phi,TDC,n}(f)$, the in-band correlated noises are not being cancelled as (4). For the uncorrelated noise, the transfer function is same as that of (4). Therefore, the FNCP increases the out-of-band noise as shown in Fig. 6(a) and (b), while not cancelling the in-band portion. The total PN spectrum of FNCP from the TDC noise is

$$S_{\phi,FNCP}(f)|_{TDC,n} = \left|1 + \frac{H_{ZOH}(f)}{H_{OL}(f)}\right|^2 \cdot S_{\phi,MP}(f)|_{TDC,n} + |H_{ZOH}(f)|^2 \cdot \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,MP}(f - k \cdot f_{ref})|_{TDC,n}. \quad (9)$$

C. Total noise

Remaining noise source is the reference noise. Using the same principle as (4), the output PN spectrum of MP and FNCP due to reference noise can be written as

$$S_{\phi,MP}(f)|_{REF,n} = S_{\phi,REF,n}(f) \cdot \left|\frac{N \cdot H_{OL}(f)}{1+H_{OL}(f)}\right|^2, \quad (10)$$

$$S_{\phi,FNCP}(f)|_{REF,n} = |1 - H_{ZOH}(f)|^2 \cdot S_{\phi,MP}(f)|_{REF,n} + |H_{ZOH}(f)|^2 \cdot \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,MP}(f - k \cdot f_{ref})|_{REF,n}, \quad (11)$$

where N is the frequency command word. The contribution from reference clock in the proposed design has <-8dBc/Hz contribution on the output noise compared to that of DCO or TDC. Therefore, the foregoing analysis assumes that the DCO random noise and TDC quantization noise are the only noise sources contributing to the output spectrum. The total noise of FNCP is approximately the sum of (4) and (9), which is

$$S_{\phi,FNCP}(f) = S_{\phi,FNCP}(f)|_{TDC,n} + S_{\phi,FNCP}(f)|_{DCO,n}. \quad (12)$$

As observed from Sections II.B and II.C, FNCP reduces the overall noise contribution from DCO but increases the contribution from TDC. Therefore, the effect of FNC on the total noise performance depends on the relative levels of the two noises. When DCO noise dominates MP PN as in Fig. 6(a) and (c), FNCP reduces the overall noise level. This can be understood intuitively in the time domain. As shown in (c), when random jitter of MP output is much larger than the resolution of FNC correction, the abrupt phase corrections hide inside the random jitter, improving the jitter performance. When TDC noise dominates, however, the correction of FNCP

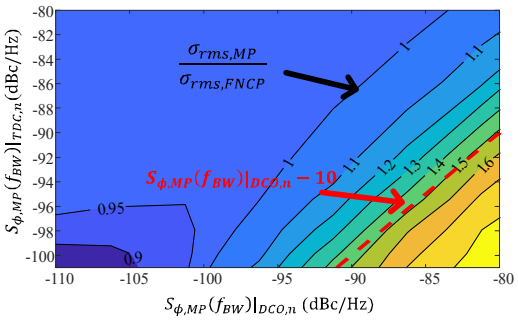


Fig. 6. Contour plots of jitter improvement by FNC with MP with regard to in-band PN level due to DCO (x-axis) and TDC (y-axis).

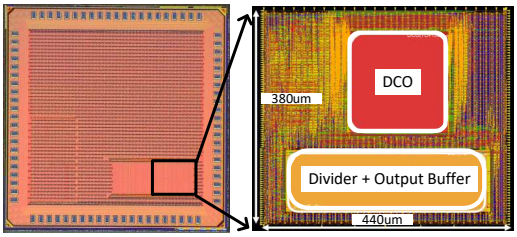
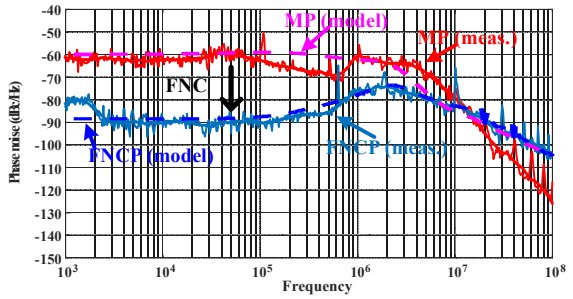


Fig. 7. Die micrograph and layout of the proposed PLL

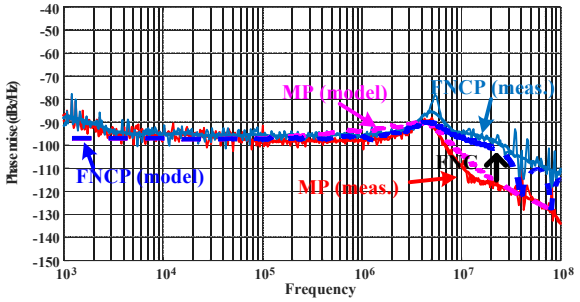
outlies the random jitter, adding more noise to the MP as shown in Fig. 6 (d). In the frequency domain, this appears as an increase in the out-of-band noise from TDC, as shown in Fig.6 (b). Fig. 7 shows a contour plot of the relationship between the jitter ratio of two modes, $\sigma_{rms,MP}/\sigma_{rms,FNCP}$, and the in-band PN level of MP due to DCO and TDC noise. The jitter values are results of behavioral simulation with $f_{ref} = 40MHz$, $f_{out} = 840MHz$, BW = 2.8MHz, sweeping ΔT_{TDC} and DCO noise level (assuming $1/f^2$ degradation). We can observe that the FNC has more effect with larger noise contribution from DCO and less from TDC. The difference should be approximately 10dBc/Hz or greater for FNC to have more than 1.5x of improvement.

III. Implementation and Results

A test chip was fabricated in 65nm CMOS technology. The layout of the PLL is done by APR tool, where the auxiliary cells are designed manually but then placed and routed automatically. Fig. 7 shows the die photo of fully-synthesized SoC and the layout of the PLL. The PLL is measured in two different modes: 1) High DCO noise, and 2) Low DCO noise. For each environment, the phase noise plots of MP and FNCP are compared in Fig. 9 along with the analytical model results. In the first case, f_{ref} = 20MHz, f_{out} = 800MHz. From Fig. 8 (a), we can observe that FNCP reduces the in-band phase noise by 15dBc/Hz at frequency offset of 1MHz, and the integrated jitter (1K – 10MHz) by 4.22x (291.8ps → 69.0ps), for only a 3.54% increase in power (7.07→7.32 mW). On the second case with low DCO noise, f_{ref} = 40MHz, f_{out} = 840MHz and the power increased from 8.78mW to 9.05mW. As we can see from Fig. 8 (b), TDC quantization noise dominates the PLL noise and the FNCP increases the out-of-band noise compared to the main



(a)



(b)

Fig. 8. Phase noise plot of measured result (meas.) and analytical model (an.) when (a) DCO noise dominates (noisy supply) (b) TDC noise dominates

path, increasing the integrated jitter (10.3ps → 18.6ps). The analytical model follows the overall tendency of the measurement results and accurately predicts both cases, verifying the frequency domain analysis of section II.

IV. Conclusions

A novel calibration-free feedforward implementation method for synthesizable ADPLL is proposed. The effect of FNC depending on the dominant noise sources are analyzed with frequency domain model and the results are compared with measurements. The condition for the proposed FNC method to be beneficial is derived.

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